Optimization of a Low Noise Amplifier Using an Interactive Evolutionary Tool

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***Abstract*—Nowadays, much of the wireless communications band at high frequencies is occupied due to the high demand of communications services, making it more and more expensive. Then, aiming to solve communications problems and use properly the available band, it's necessary to use high technology software and hardware. Radio frequency (RF) circuits on transmitters and receivers of a communication system can be modified to improve the performance. However, the design of RF circuits is difficult, time-consuming and based on designer knowledge and experience. This work proposes an evolutionary approach using the genetic algorithm, which is implemented in the in-house iMTGSPICE optimization tool, to perform the optimization process of a robust (corner and Monte Carlo analyses) Low Noise Amplifier (LNA) in a 130 nm Bulk CMOS technology.**

Keywords— Computer-aided design (CAD), genetic algorithm, radio frequency, low noise amplifier (LNA).

I. INTRODUCTION

The diversity of wireless communications applications has increased over the last years with concepts such as Internet of Things (IoT) and Industry 4.0. They simplify and improve the monitoring and controlling of systems. However, with the increase of diversity the demand increases too, which makes the available communication band narrower and noisier. A basic approach to overcome the noise problem is to improve the circuit at the receiver of the communication system. The LNA is the first active building-block in a reception chain [8], [9]. and one of most important circuits at the receiver, which can be implemented using Complementary Metal-Oxide-Semiconductor (CMOS) technology. They are responsible for amplifying the received analog signal in order to add minimal noise as much as possible [15].

RF circuits are traditionally designed by hand, based on circuit behavioral equations, followed by an iterative manual process using electrical circuit simulators. This process is often very difficult, costly, time-consuming and dependent on designer's experience [1], [2]. Moreover, the optimization processes of RF CMOS ICs which are performed by manual methods usually require much knowledge and experience of the designers to reach the additional metrics required by this kind of ICs. Consequently, the complexity presented by RF CMOS ICs complicates its automation task, and, therefore, its design has remained dependent on the expertise of RF designers.

In this scenario, the trend of the optimization processes of robust (corner and Monte Carlo analyses) analog and RF CMOS ICs are based on evolutionary computation techniques [3], [4], [5]. To overcome this complex and challenging issue, this work proposes the use of an in-house computational tool to optimize RF CMOS ICs, named iMTGSPICE [6], [7]. It can reduce the optimization cycle-times (OCTs) of these circuits due to its heuristic processes of artificial intelligence. Furthermore, it performs the corner and Monte Carlo analyses in the loop of optimization process without reducing the sample space of searching. However, by the proposed approach, the OCT is feasible, considering all time considered for the optimization of these types of circuits. Therefore, by using iMTGSPICE, the designers can meet severe specification in a reduced OCT, while guaranteeing the robustness of analog and RF CMOS ICs, considering the environmental and manufacturing process variations.

In order to validate the proposed computational tool, a classical project using RF LNA is redesigned using a new topology and technology. The proposed iMTGSPICE tool is used for the optimization process. The obtained results are compared with another work in terms of RF figures of merit (FoMs) aiming to assess the capability of the proposed methodology in relation to migration of classical RF designs to novel technologies and RF topologies.

This paper is organized as follows: Section 2 presents the approach proposed in this work. Next, in Section 3, the LNA topology used in this work is presented. The LNA specifications and configuration parameters of the optimization framework are provided in Section 4. Section 5 discusses the results achieved by the proposed approach and compares with

another work. Finally, Section 6 draws the conclusions obtained in this work.

II. Evolutionary Methodology

Figure 1 illustrates the flowchart of the evolutionary approach with the genetic algorithm (GA) proposed, entitled iMTGSPICE [6], [7]. It is developed in C++ language and manages the Spice Opus simulator [9]. This optimization tool performs the robustness analyses of Corner (CA) and Monte Carlo (MCA) in the loop of the optimization process.

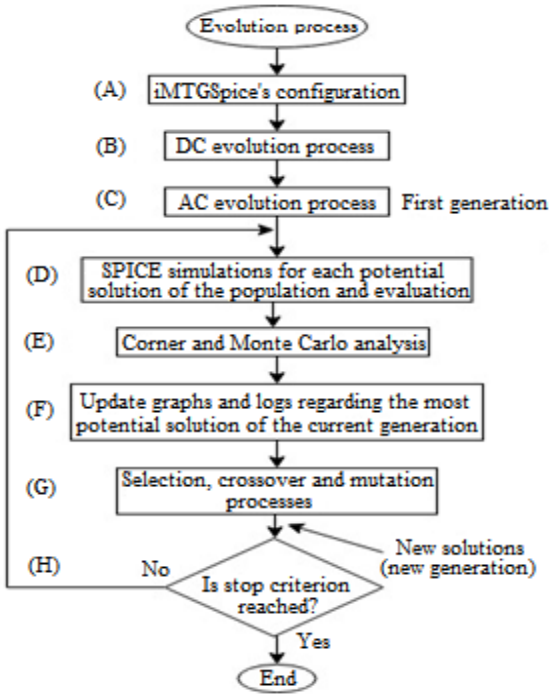

Figure 1: Flowchart of iMTGSPICE.

At the start of the optimization process, the designer must configure the iMTGSPICE (Block A) [7], [11]: the description of the circuit (SPICE *netlist* for DC and AC analysis); input variables with their desired ranges; the output variables, which are the desired specifications or FoMs with their respective tolerance ranges; the GA parameters, such as population size (N_P), crossover and mutation rates (P_C and P_M), the weight (priority) applied for each FoM of the fitness function (We_i), where i is an index that represents a FoM, σ is the standard deviation of the Gaussian fitness functions [11], and N_{Rob} is the desired number of solutions contained in the population that fully meet the design specifications through the robustness analyses, which is used as the stop criterion.

The evolution process is performed in two stages [11], [12]. The first stage (Block B) is responsible for evolving the direct current (DC) bias conditions of the MOSFETs, to ensure that all of them operate in the desired saturation region. The second stage (Block C) is responsible for making the evolution process of the alternating current (AC) analysis of the analog CMOS ICs. It generates randomly a set of N_P potential solutions and replaces some of them by the best solutions found in the first stage of the evolution process (DC stage).

Next, in Block D, each potential solution is simulated in SPICE [11]. Then, the specifications of each potential solution are obtained and evaluated by minimization, center value, and maximization fitness functions [11] considering a range from 0 to 100.

Afterwards, in Block E, the robustness of the best potential solutions evaluated by the fitness function are calculated, until the evolution process finds the N_{Rob} robust potential solutions. The robustness calculation regarding a potential solution is performed as follows: I- the deviations of the different FoMs found in relation to their minimum and maximum values of the desired specifications; II- the average value of the deviations found of item I (ε_{sol}), regarding the smallest values of them (worst performance of each FoM, considering their minimum and maximum values) [7]. Next, the value of the fitness function of each potential solution is calculated considering the value of its ε_{sol}. Afterwards, the population is reordered, giving the highest priority for the most robust potential solutions, which are identified by those that more maximize the FoMs (highest ε_{sol} values).

The FoMs, MOSFETs' dimensions, bias conditions, and values of the passive components of the most robust potential solution obtained is displayed in the screen of iMTGSPICE (Block F). Figure 2 presents one of the screens, which is monitoring the $Eval_{Sol}$ and FoMs found, considering the CA and MCA in the loop of the optimization process as a function of the number of iterations.

Next, in Block G, genetic operators [7] are applied to generate a new population to be evolved [7]. The selection process of the best robust potential solutions is performed by the binary tournament. Afterwards, the single-point crossover is applied for the selected individuals in population to generate a new set of individuals for the next generation, and finally a bit flip mutation is applied for this new generation to further explore the search process of potential solutions. The stop criterion is verified in Block H. If the desired number of robust solutions (N_{Rob}) is achieved the optimization process finalizes, otherwise it continues until reaching N_{Rob} or the maximum number of iterations defined by the designer.

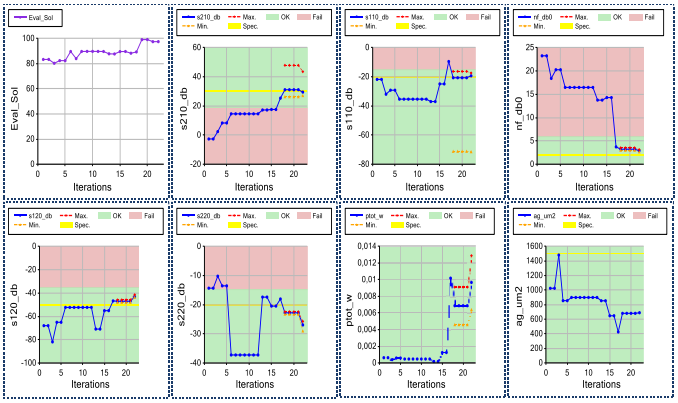

Figure 2: Screen of iMTGSICE which shows the monitoring of the the $Eval_{Sol}$ and FoMs obtained by the best potential solution in each generation of the optimization process.

III. The LNA Topology

The LNA that was proposed is presented in Figure 3. It is based on an ultra-low power LNA first presented by [9]. The LNA is composed of two stages. The first stage implements a classical self-biased inverter, followed by a buffer stage [9].

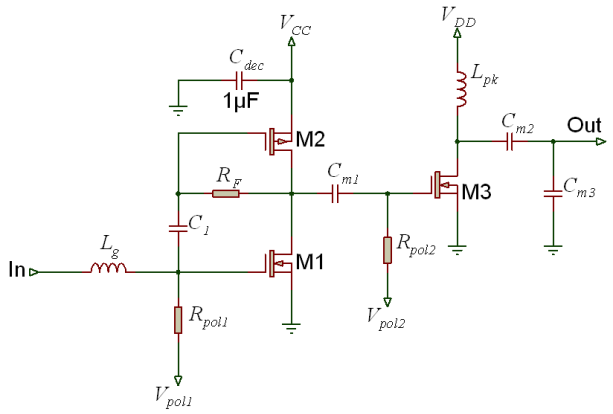

Figure 3: Topology of the LNA.

In Figure 3, V_{CC} and V_{DD} are fixed supply voltages. The input terminal is represented by *in* node and the output terminal by the *out* node. M1 (nMOSFET) and M2 (pMOSFET) compose the self-biased inverter and M3 (nMOSFET) compose the buffer stage. The LNA is also composed of passive components: resistors (R_F, R_{pol1}, R_{pol2}), inductors (L_g and L_{pk}) and capacitors (C_{m1}, C_{m2}, C_{m3}, C_1). The large decoupling capacitor, C_{dec}, ensures AC ground at the PMOS source. Finally, V_{pol1} and V_{pol2} are bias voltages to be optimized in this work to achieve the desired LNA specifications.

IV. The LNA Specifications and Configuration Parameters

In this work, we have considered the desired specifications of the LNA in Table I.

TABLE I. The Desired Specifications of the LNA

Figures of merit	Specifications
$\|S_{21}\|$	$\geqslant$ 19 dB
$\|S_{11}\|$	$\leqslant$ -15 dB
$\|S_{12}\|$	$\leqslant$ -35 dB
$\|S_{22}\|$	$\leqslant$ -15 dB
NF	$\leqslant$ 6 dB
P_{TOT}	$\leqslant$ 20 mW

Regarding Table I, S_{21} is the forward gain, S_{11} and S_{22} are the input and output reflection coefficients, respectively, S_{12} is the reverse isolation, *NF* is the noise figure, P_{TOT} is the power consumption and A_G is the gate area of the MOSFETs. Moreover, all MOSFETs (M1, M2 and M3) are set to operate in the saturation region (functional constraints). Additionally, in this work, the LNA operates at 900 MHz under 1.2 V supply voltages V_{CC} and V_{DD} and the nominal operating temperature of the LNA is 27°C. The manufacturing process used to implement the LNA is the 130 nm Bulk from the GlobalFoundries [13].

Table II presents the ranges of values adopted for the optimization parameters (minimum, maximum, and step size values) for the evolution processes of the LNA [11].

TABLE II. The Optimzation Parameters of the LNA

Design Parameter	Range
W	[0.13, 100, 0.1] µm
L	[0.13, 50, 0.1] µm
R_F	[100, 20k, 1] Ω
R_{pol1}	[100, 30k, 1] Ω
R_{pol2}	[100, 15k, 1] Ω
L_g	[5, 20, 0.1] nH
L_{pk}	[1, 10, 0.1] nH
C_{m1}	[0.1, 5, 0.05] pF
C_{m2}	[0.5, 5, 0.05] pF
C_{m3}	[0.5, 5, 0.05] pF
C_1	[5, 20, 0.05] pF
V_{pol1}	[0.4, 1.2, 0.05] V
V_{pol2}	[0.4, 1.2, 0.05] V

Note: the ranges of the parameters mean [minimum value, maximum value, and step size value].

Initially, the default values for the weights (We_i) of the fitness function of all FoMs were considered the same to perform the evolution process regarding the DC evolution process (first stage), that is, 50% for P_{TOT} and A_G. Similarly, regarding the AC evolution process (second stage), we considered the same weights for the FoMs ($|S_{21}|$, $|S_{11}|$, $|S_{12}|$, $|S_{22}|$, *NF*, P_{TOT}, and A_G). Moreover, the σ parameter of the Gaussian fitness function was set to 0.2 for all profiles considered (minimization and maximization) and the two evolution processes, which is related to a maximum tolerance of 25% for the desired specifications [11].

It is important to mention that the CA is performed first, and subsequently, the MCA is performed only for those potential solutions that met all desired specifications found by the CA. This procedure is performed to avoid waste of time in the MCA when a certain potential solution is not robust by the CA, considering that the aim of the optimization process is to ensure the design robustness by both analyses simultaneously.

V. Results

The iMTGSPICE was run in a 2.2 GHz Notebook with 8 GB RAM and Windows 10 (operating system). The

optimization process, taking into account robustness analyses (CA and MCA), took 38 minutes to find robust solutions.

Table III presents the design variables, and Table IV the average values of the FoMs obtained.

TABLE III. DESIGN VARIABLES FOR THE LNA

Design Variables		
W_1 = 62.0 µm	R_f = 16584 Ω	C_{m1} = 1.4 pF
W_2 = 57.5 µm	R_{pol1} = 663 Ω	C_{m2} = 4.2 pF
W_3 = 74.8 µm	R_{pol2} = 4972 Ω	C_{m3} = 4.1 pF
L_1 = 3.8 µm	L_g = 5.5 nH	V_{pol1} = 1.10 V
L_2 = 20.1 µm	L_{pk} = 7.6 nH	V_{pol2} = 0.68 V
L_3 = 0.4 µm	C_1 = 19.3 pF	

TABLE IV. THE OPTIMIZATION PARAMETERS FOR THE LNA

FoMs	**Obtained FoMs**	
	This work	**[14]**
$\|S_{21}\|$	33.8 dB	19.1 dB
$\|S_{11}\|$	-23.3 dB	-15.7 dB
$\|S_{12}\|$	-50.1 dB	-43.5 dB
$\|S_{22}\|$	-23.1 dB	-20.0 dB
NF	4.93 dB	2.78 dB
P_{TOT}	10.1 mW	18.9 mW

We can observe in Table III that the iMTGSPICE achieved successfully the specifications within the desired tolerance range. Although the noise figure resulted 77.3% higher than [14], this work obtained the best results for most FoMs, with significant improvements of 77.0%, 48.4% and 46.6% for voltage gain, input reflection coefficient and power consumption, respectively. However, it must be emphasized the fact that different LNA topologies and CMOS technologies were used, and a very important information was absent in the original reference, the robustness regarding manufacturing process and environmental conditions.

VI. CONCLUSION

This paper proposed an approach using genetic algorithm to optimize RF CMOS ICs, which was integrated to the in-house optimization tool named iMTGSPICE. A classical project using RF LNA was redesigned using a new topology and technology in order to validate the proposed approach. The results showed that this tool, through the evolutionary algorithm method, and Corner and Monte Carlo analysis, is capable of produce robust solutions, with a low optimization process time (38 minutes). Therefore, the iMTGSPICE demonstrated to be a reliable tool to design RF CMOS integrated circuits and migrate classical RF designs to new technologies and RF topologies.

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